RESISTIVE VIAS FOR CONTROLLING IMPEDANCE AND TERMINATING I/O SIGNALS AT THE PACKAGE LEVEL

BACKGROUND OF THE INVENTION

[0001] Circuit package designs are utilizing higher operational frequencies to satisfy data rate increases of integrated circuits. As a result, package designs must address challenges to signal propagation presented by the increased operational frequencies that were previously ignored, such as distributed resistance and capacitance (RC) of the conductor, an impedance of the driving source and load impedance. Specifically, for very long conductors, i.e., conductors whose length is great compared to the wavelength of a signal, the RC of the conductor produces propagation delays, as well as contributes to impedance mismatches. Impedance mismatch between the driving source and the conductor results in signal reflection, which interferes with signals produced by the driving circuit, typically referred to as return loss. Return loss results in both noise and shape degradation in signals produced by the driving circuit.

[0002] To avoid impedance mismatch, packages may be designed with discrete resistors to define the impedances of the signal lines connected to the driving receiving circuit. Typically, these discrete resistors are formed by printing, such as screen printing, a thick-film resistive paste or ink on a substrate and are referred to as thick-film resistors. The predictability and variability (or tolerance) of the electrical resistance of a thick-film resistor has proved challenging.

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[0003] As a result, circuit package design typically has depended upon integrated circuit design to solve the

problems presented by high frequency signal propagation. For example, United States patent number 6,115,298 to Kwon et al. discloses a semiconductor device to that includes a circuit to reduce impedance mismatch between the semiconductor device and a bus connected thereto. The bus consists of a plurality of signal lines. The semiconductor device includes a discrete resistor, corresponding to the impedance of the signal lines. The signal lines are connected to a plurality of second pads. A reference voltage generator generates a reference voltage. A comparator compares a voltage on the first pad with the reference voltage, generating a control signal in response to the comparison. A code generator generates a code signal in accordance with the control signal to produce a current on the first pad. A data driver drives data signals to the signal lines connected to the second pads according to the code signal, thereby matching the impedance of the data driver with the impedance of the signal lines.

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[0004] United States patent number 5,808,478 to Andresen discloses a buffer with a slew rate that is load independent. The buffer is comprised of an output buffer connected to an output terminal. The output buffer is controlled such that it can drive a load with different drive levels by changing the transconductance internal thereto. The transition on the input to the buffer is passed through an intrinsic delay block and variable delay block to provide a delay signal on a node. A first phase detector latch with a first threshold voltage compares this transition with the transition on the output terminal. A second phase detector latch with a second threshold voltage, also compares this delayed transition with that on the output terminal. If both of

the latches indicate that the delayed transition occurred after the transition on the output terminal, a control signal on a line is changed by incrementing a counter. This will change the drive to a load. If the transition on the output terminal occurs after the delayed transition, then the counter increments the count value in the opposite direction, increasing the drive to the load to increase the speed of the output driver.

[0005] What is needed, however, is a circuit package design that minimizes impedance mismatch between the driving source and the conductor.

SUMMARY OF THE INVENTION

[0006] Provided is a circuit package and a method of forming the same that facilitates control of the impedance of a driving circuit employing resistive vias formed into a dielectric substrate. In this manner, the input impedance, output impedance or both of the driving circuit may more closely match the impedance of the conductor, or transmission line, of a package that is connected thereto. To that end, the package includes a dielectric substrate having a first surface and a second surface, disposed opposite to the first surface. A via extends between the first and second surface, and a first conductor is disposed on the surface that extends from the via. A second conductor is disposed on the second surface and extends from the via. The via has a resistive fill disposed therein, defining a resistance connected between the first and second conductors. A driver circuit is mounted to the substrate and includes an input and an output. The output is in electrical communication with the first conductor and has an output impedance associated therewith. The output impedance

includes an output resistive component and an output reactance component. The output resistive component including the resistance, and the resistance is of sufficient magnitude to be the dominant component of the output impedance. In another embodiment, the impedance of the input is controlled in a similar fashion. The method defines steps to make the aforementioned circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Fig. 1 is a schematic illustrating the structure of the circuit in accordance with the prior art:

[0008] Fig. 2 is a schematic illustrating the structure of the circuit in accordance with the present invention;

[0009] Fig. 3 is a cross-sectional view showing the circuit of Fig. 2 implemented in a circuit package in accordance with the present invention;

[0010] Fig. 4 is a schematic illustrating the structure of the circuit in accordance with an alternate embodiment of the present invention;

[0011] Fig. 5 is a cross-sectional view showing the circuit of Fig. 4 implemented in a circuit package in accordance with the alternate embodiment of the present invention; and

[0012] Fig. 6 is a cross-sectional view showing the circuit of Fig. 4 implemented in accordance with a second alternate embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Referring to Fig. 1 a prior art circuit 10 is shown including a driver circuit 12 connected to a conductor, or transmission line, shown as line segments 14a and 14b and an output match resistor Rm_{output} connected to the transmission line proximate to output 18. Driver circuit 12, in this example, is a buffer with an input 16 and an output 18. In this first implementation, output match resistor Rm_{output} is connected to both output 18 and transmission line, with the transmission line including line segments 14a and 14b. Output match resistor Rm_{output} is employed to ensure that the impedance of output 18 closely matches the impedance of the transmission line, for a given operational frequency of circuit 10. Specifically, the output impedance $R_{TOTALDRIVER}$ associated with driving circuit 12 may be defined as follows:

$$1. \quad R_{TOTALDRIVER} = Rm_{OUTPUT} + R_{DRIVER}$$

where R_{DRIVER} is the output resistance at output 18.

[0014] Varying the value of R_{DRIVER} is the most efficient manner by which to adjust $R_{TOTALDRIVER}$. However, adjusting R_{DRIVER} internal to driving circuit 12 is problematic for several reasons. Firstly, silicon process control, effective voltage at transitors, and temperature makes it extremely difficult to determine the magnitude of R_{DRIVER}, since R_{DRIVER} could vary 50% or even more. In addition, driving circuit 12 is typically an off-the-shelf item that is already fabricated, affording very little opportunity to modify the resistive component of the output impedance when being implemented in a package design. The presence of output match resistor Rm_{output} facilitates control of the value $R_{TOTALDRIVER}$.

Furthermore, the presence of line segment 14a may eliminate any benefit of using Rm_{output} if line segment 14a is long enough to be a transmission by introducing reflections caused by impedance mismatches.

[0015] Referring to Fig. 2, to accurately control the impedance of output 118, output match resistor Rm_{output} is preferably coupled to the transmission line proximate to output 118. To that end, the connection between Rm_{output} is made proximate to output 118 so that the impedance attributable to transmission line segment 14a, shown in Fig. 1, is abrogated. As a result circuit 110, of Fig. 2, has output 118 directly connected to Rm_{output}, with the opposing end of Rm_{output} being connected to transmission line segment 114b. To further improve impedance matching, magnitude of the resistance of match resistor is selected so that it becomes the dominant component of term for $R_{TOTALDRIVER}$ and ensures an impedance match between output 118 and the transmission line. To that end, and in accordance with the present invention, the relationship between Rm_{output} and R_{DRIVER} being defined as follows:

$$2. \quad Rm_{output} > R_{DRIVER}$$

In this manner, the impedance of output 118 may be closely matched, within very tight tolerances, to the impedance of the transmission line that is defined by line segment 114b. Exemplary resistance values for R_{DRIVER} are in a range of 5 to 12 ohms, inclusive. Output match resistor Rm_{output} has a value that is no less than twice the value of R_{DRIVER} and is typically in a range of 35 to 50 ohms, inclusive.

[0016] Referring to Fig. 3, implementing circuit 110 in a package 20, however, poses certain challenges in obtaining an accurate value of output match resistor Rm_{output} due to the limitations of thick-film technology as set forth above. As shown, package 20 includes a dielectric substrate, or body 21, having a first surface 21a and a second surface 21b, disposed opposite to first surface 21a. Driver circuit 112 is coupled to conductive traces 21c on surface 21a employing conductive bumps, 112a, typically employed in flip-chip attachment techniques. Located between first and second surfaces 21a and 21b are a plurality of spaced-apart and parallel conducting planes, shown as 21d, 21e and 21f contained therein with vias 22, 23, 24, 25 and 26 extending from a surface of dielectric body 21a down to differing conducting layers 21d, 21e and 21f. These conducting layers may serve any function desired, such as power, ground or signal lines. For purposes of the present discussion, conducting planes 21d, 21e and 21f are discussed with the function of a signal transmission line. To improve the impedance match between output 118 and one of the transmission lines, in this example conducting layer 21a, output match resistor Rm_{output} is formed by filling via 22 with a resistive material. Via 22 is selected to be spatially more proximate to output 118, compared to the remaining vias, e.g., vias 23 and 24. In this manner, the value of the resistance of output match resistor Rm_{output} may be ensured to comprise the dominant components of the impedance at region of circuit 110 where output match resistor Rm_{output} is present. This enables concurrently establishing an output resistance component of $R_{TOTALDRIVER}$ and matching the characteristic impedance of the transmission line Z_0. In

this manner, the impedance of output 118, $R_{TOTALDRIVER}$, is made to closely match the impedance of transmission line, Z_0.

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[0017] Referring to both Figs. 4 and 5, although the foregoing has been explained with respect to controlling the impedance at output 118, $R_{TOTALDRIVER}$, the same holds true for the impedance at input 116, R_{input}, used as a pull-up and termination voltage resistor. To that end, a termination resistor Rm_{input} is connected to both input 116 and a power plane at plane 21f. Termination resistor Rm_{input} is formed by introducing resistive fill in via 25 and has a value selected so that it matches the characteristic impedance, Z_0, of transmission line 114b. This properly terminates signal arriving at input 116. Additionally, were other inputs or outputs (I/Os) present on driver 112, shown as I/O 127, may be connected to a resistive via, such as 26, in order to achieve impedance matching between I/O 127 and conductive plane 21e. It should be noted that the value of the resistors defined by filling vias 22, 25 and 26 with resistive material may be controlled by varying the dimensions of the vias, employing resistive fill with differing resistivity or both. As a result a great amount of flexibility is provided with not only matching the impedance between driver I/Os, but also ensuring that the resistivity provided by vias 22, 25 and 26, are identical.

[0018] Referring to Fig. 6, were it desired to reduce the resistive component of $R_{TOTALDRIVER}$ without changing the resistive properties of the resistive fill, then via 23 and/or via 24, could be filled with a resistive fill to create an additional resistance by formation of Rm_{output}'. Assuming Rm_{output} and Rm_{output}' have substantially similar

volumes, this would reduce the resistive component associated with $R_{TOTALDRIVER}$. However, the actual values of Rm_{output} and Rm_{output}' would be selected to avoid impedance mismatches between output 118 and the transmission line.

[0019] Although the foregoing has discussed the circuit driver 112 as comprising a buffer, it should be understood that driver circuit 112 may be any type of active circuit known in the electrical arts, such as an inverter, an amplifier and the like. Further, where the foregoing has been described with respect to flip-chip technology, it should be understood that the present invention applies to other packaging designs, e.g., printed circuit boards (PCB). To that end, substrate 21 may be a printed circuit board and conductive bumps 112a may be solder balls. Therefore, the scope of the invention should not be based upon the foregoing description. Rather, the scope of the invention should be determined based upon the claims recited herein, including the full scope of equivalents thereof.